

# USB4 1.0 ENGINEERING CHANGE NOTICE FORM

**Title: Adding Minimum SLOS Time on CLx Exit**  
**Applied to: USB4 Specification Version 1.0**

<b>Brief description of the functional changes:</b>
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Adding a requirement for minimum SLOS transmission after detecting conditions to transition to the next state in the Lane Initialization and CL0s, CL1 and CL2 flows on Gen 2 and Gen 3
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<b>Benefits as a result of the changes:</b>
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Allowing a Re-timer to lock on the SLOS signal on Lane Initialization and exiting CLx
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<b>An assessment of the impact to the existing revision and systems that currently conform to the USB specification:</b>
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None
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<b>An analysis of the hardware implications:</b>
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None
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<b>An analysis of the software implications:</b>
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None
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<b>An analysis of the compliance testing implications:</b>
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Adding a check for Routers and verify SLOS is transmitted for at least tTxSLOS time
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## Actual Change

### (a). Table 4-32 – Gen 2 and Gen 3 Training Sub-State Machine Transitions

#### To Text:

Transition	From State	To State	Conditions <sup>1</sup>
1	LOCK1	LOCK2	<ul style="list-style-type: none"><li>Received 2 SLOS Symbols (SLOS1 and/or SLOS2) in a row.</li><li>Sent at least 2 complete SLOS1</li><li>Receiver completed TxFFE negotiation (i.e. <i>Rx Locked</i> = 1b).</li></ul>
2	LOCK2	TS1	<ul style="list-style-type: none"><li>Received 2 SLOS2 Symbols in a row.</li><li>Sent at least 2 complete SLOS2<ul style="list-style-type: none"><li>It is recommended to count the transmitted SLOS2 after receiving 2 SLOS2 Symbols in a row.</li></ul></li></ul>

### (b). Section 4.2.1.6.5.1.1 – Gen 2 and Gen 3 Exit Flow from CL0s State

#### To Text:

- On detection of 2 back-to-back TS2 Ordered Sets, continue sending SLOS1 for tTxSLOS time, then stop sending SLOS1 and send at least 16 TS2 Ordered Sets. The first TS2 Ordered Set shall be sent within tTrainingTransition after detection of the second TS2 Ordered Set.

### (c). 4.2.1.6.5.3 – Gen 2 and Gen 3 Exit flow from CL1 or CL2 state (Retimers on the Link)

#### To Text:

- Upon reception of 7 back-to-back CL\_WAKE2.X Ordered Set Symbols or 7 back-to-back SLOS Symbols, continue sending SLOS1 for tTxSLOS time, then transition the Adapter to Training.LOCK1 sub-state within tWakeResponse time.

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- Upon reception of 7 back-to-back CL\_WAKE2.X Ordered Set Symbols or 7 back-to-back SLOS Symbols, continue sending SLOS1 for tTxSLOS time, then transition to Training.LOCK1 sub-state.

### (d). Table 4-72 – Logical Layer Timing Parameters

#### To Text:

Parameter	Description	Min	Max	Units
<u>tTxSLOS</u>	<u>Time to continue sending SLOS after detecting the conditions to send next Ordered Sets TS1 or TS2.</u>	<u>200 (Gen 2)</u> <u>100 (Gen 3)</u>	=	<u>ns</u>

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## (e). Changes in the Re-timer Specification

### Gen 2 and Gen 3 Clock Switch Flow

The transmitters shall stop using the local clock and shall start using the recovered clock from the Corresponding Receiver. The transition may or may not take place on Symbol boundary.

After a transmitter switches to using the receiver clock, it shall forward the bit stream it receives from the Corresponding Receiver instead of transmitting its locally-generated patterns. If there is more than one Re-timer on the Link, the Channel's receiver may lose alignment during the Clock Switch flow of other Re-timer(s). The Re-timer shall complete Symbol Realignment of the SLOS Ordered Sets within tSymbolLockRT time. The Re-timer shall set the *Clock Switch Done* bit in the Corresponding Receiver to 1b. Figure 4-3 shows how the *Clock Switch Done* bits are set.

### CL0s Exit Flow

After a Re-timer receives 3 back-to-back CL\_WAKE2.X Symbols (where X is the same value as in step 4) on at least one Lane Adapter, the Re-timer shall transition each Re-timer Channel that is in CL0s state to transmit on the clock recovered from the received Symbols rather than on its local clock.

- The transition shall happen only after bit lock is achieved by all Re-timer Channels that are in CL0s state.
- The transition may or may not take place on Symbol boundary.
- Each Re-timer Channel in CL0s state shall transition to Forwarding state. From this point on, a Re-timer Channel shall forward the bit stream it receives from the Lane and stop generating CL\_WAKE1.X Symbols.
- During the transition from local clock to receiver clock, the Re-timer shall meet the SSC\_SLEW\_RATE requirement as specified in the USB4 Specification.

After the Re-timer Channels transitioned to Forwarding state, the Channel's receiver will receive SLOS Ordered Sets. The Re-timer shall complete Symbol Realignment of the SLOS Ordered Set within tSymbolLockRT time.

### CL1/2 Exit Flow

#### **4.2.4.3.1.3 Timing Requirements**

A Re-timer shall meet the following timing requirements during exit from CL0, CL1, or CL2 states:

- A receiver shall complete Symbol lock within tCLxLock of receiving SLOS or CL\_WAKE1.X Symbols.
- A transmitter shall complete the transition to a recovered clock within tSwitchNoSSC if the received clock is a non-SSC clock.
- A transmitter shall complete the transition to a recovered clock within tSwitchSSC if the received clock is an SSC clock.
- A receiver shall complete Symbol Realignment within tSymbolLockRT after Ordered Sets changes.

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**Table 4-6. Re-timer Timing Parameters**

Parameter	Description	Min	Max	Units
<u>tSymbolLockRT<sup>1</sup></u>	<u>Time to complete Symbol Realignment when receiving SLOS on Lane Initialization and CL0s, CL1 and CL2 exit flows</u>		<u>400 (Gen 2)</u> <u>200 (Gen 3)</u>	<u>ns</u>
<p><u>Notes:</u></p> <p><u>1. On-board Re-timer may use higher values of tSymbolLockRT if the Router in the assembly provides sufficient time for the Re-timer to lock. Given tLatency2/3 of the On-board Re-timer and tTrainingTransition and tSymbolLock of the Router of the assembly, the tSymbolLockRT of the Re-timer should be:</u></p> <p><u><math>tSymbolLockRT &lt; 2 * tLatency2/3 + tSymbolLock + tTrainingTransition + 10ns + 90ns * (4 - Gen)</math></u></p>				